EXHIBIT 5

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INPHI CORPORATION
Requester 1,

SMART MODULAR TECHNOLOGIES (WWH), INC.
Requester 2, and

GOOGLE INC.
Requester 3

v.

Patent of NETLIST, INC.
Patent Owner

Appeal 2015-006849
Merged Reexamination Control Nos. 95/001,339, 95/000,578, and 95/001,579
Patent 7,619,912 B2
Technology Center 3900

Before JEFFREY B. ROBERTSON, DENISE M. POTHIER, and JEREMY J. CURCURI, *Administrative Patent Judges*.

POTHIER, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Requesters 1–3 made three separate requests for *inter partes* reexamination of U.S. Patent No. 7,619,912 B2 ("the '912 patent") issued to Jayesh R. Bhakta and Jeffrey C. Solomon, entitled *Memory Module Decoder*. The '912 patent issued November 17, 2009 and is assigned to Patent Owner, Netlist Inc. Requestor 1 requested reexamination of claims 1–51 of the '912 patent, which was assigned Control No. 95/001,339; Requester 2 requested reexamination of claims 1, 3, 4, 6–11, 15, 18–22, 24, 25, 27–29, 31–34, 36–39, 41–45, and 50 of the '912 patent, which was assigned Control No. 95/000,578; Requester 3 also requested reexamination of the same claims of the '912 patent as Requester 2, which was assigned Control No. 95/000,579. R1 Request 6; R2 Request 1; R3 Request 1.[1] On February 28, 2011, Control Nos. 95/001,339, 95/000,578 and 95/000,579 were merged into a single proceeding. Dec. *Sua Sponte* to Merge Reexamination Proc. 6.

Although indicating claims 1–136[2] are subject to reexamination in the RAN, the Examiner further states claims 44, 51, 55, 59, 64–66, 72–74, 76, 94–108, and

[1] Throughout this opinion, we refer to (1) the Appeal Briefs filed by Requester 1, Requester 2, Requester 3, and Owner as R1 App. Br., R2 App. Br., R3 App. Br., and PO App. Br. respectively; (2) the Respondent Briefs filed by Owner (for Requesters 1–3), Requester 1, Requester 2, and Requester 3 as PO-R1 Resp. Br., PO-R2 Resp. Br., PO-R3 Resp. Br., R1 Resp. Br., R2 Resp. Br., and R3 Resp. Br. respectively ; (3) the Rebuttal Briefs by Requester 1, Requester 2, Requester 3, and Owner as R1 Reb. Br., R2 Reb. Br., R3 Reb. Br., and PO Reb. Br.; (4) the Examiner's Answer (Ans.) mailed January 14, 2015; (5) the Examiner's Right of Appeal (RAN) mailed June 18, 2014, (6) the Action Closing Prosecution (ACP) mailed March 21, 2014, and (7) Requests for Reexaminations by Requester 1, Requester 2, and Requester 3 as R1 Request, R2 Request, and R3 Request respectively.

[2] Claims 52-136 were added during the course of reexamination. *See* RAN 4.

112–118 have been canceled. RAN 1. Accordingly, claims 1–43, 45–50, 52–54, 56–58, 60–63, 67–71, 75, 77–93, 109–111, and 119–136 remain pending. Of those claims, claims 2, 5, 7, 9, 21, 23, 26, 30, 33, 57, and 119 have been rejected and claims 1, 3, 4, 6, 8, 10–20, 22, 24, 25, 27–29, 31, 32, 34–43, 45–50, 52–54, 56, 58, 60–63, 67–71, 75, 77–93, 109–111, and 120–136 are indicated as patentable. *Id.*

Requesters 1–3 appeal from the decision in the RAN not to adopt various rejections. R1 App. Br.; R2 App. Br.; R3 App. Br. Patent Owner filed respondent briefs. PO-R1 Resp. Br.; PO-R2 Resp. Br.; PO-R3 Resp. Br. Each Requester filed a rebuttal brief to their respective appeals. R1 Reb. Br.; R2 Reb. Br.; R3 Reb. Br.

Owner cross appeals from the decision in the RAN, rejecting claims 2, 5, 7, 21, 23, 26, 30, 33, and 119 of the '912 patent. PO App. Br. 2. Owner states that rejected claims 9 and 57 are not being appealed. PO App. Br. 47. Requesters 1–3 filed respondent briefs, and Owner filed a rebuttal brief. *See generally* R1 Resp. Br., R2 Resp. Br., R3 Resp. Br., and PO Reb. Br; *see also* Ans. 2.

The Examiner's Answer relies on the RAN, incorporating it by reference. *See* Ans. 1.

An oral hearing was conducted on November 24, 2015. A transcript has been made of record.

We have been informed that the '912 patent relates to (1) U.S. Patent Nos. 7,289,386, 7,532,537, 7,636,274, and 7,864,627 (the '386, '537, '274, and '627 patents, respectively), (2) merged reexamination Control Nos. 95/000,546 and 95/000,577 for the '386 patent, which was appealed to the Board as Appeal No. 2014-007777, and where the rejection of pending claims was affirmed on February

25, 2015,[3] (3) reexamination Control No. 95/001,381 for the '537 patent, which was appealed to the Board as Appeal No. 2013-009066 and where the Examiner's decision to confirm the patentability of the claims was affirmed on January 16, 2014,[4] (4) reexamination Control No. 95/001,337 for the '274 patent, which has been reopened based on the Board decision dated January 16, 2014 (Appeal No. 2013-009044),[5] (5) reexamination Control No. 95/001,758 for the '627 patent, which was appealed to the Board as Appeal No. 2015-007761 and was heard on December 11, 2015, (6) various AIA proceedings, including IPR2014-00882, IPR2014-00883, and IPR 2014-01011,[6] and (7) several court proceedings.[7] R1 App. Br. 1; R2 App. Br. 2, 18; R3 App. Br. 1, 65; PO App. Br. 1.

We have jurisdiction under 35 U.S.C. §§ 134(b) and 315 (2002).

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[3] Subsequent to the decision, Patent Owner and Requester 3, Google Inc., filed notices of appeal to the Federal Circuit on October 26, 2015 and October 30, 2015, respectively. On February 15, 2016, the appeal was dismissed. *Netlist, Inc. v. Google Inc.*, Nos. 16-1270 and 16-1271, slip op. at 1 (Fed. Cir. January 28, 2016).

[4] Subsequently, Requester appealed the Board decision to the Federal Circuit, which affirmed the Board's decision on November 13, 2015. *Inphi Corp. v. Netlist, Inc.*, 805 F.3d 1350 (Fed. Cir. 2015).

[5] On January 16, 2014, the Board affirmed-in-part and presented new grounds of rejection for various claims. The proceeding has been remanded to the Central Reexamination Unit.

[6] *Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-00882, Paper No. 33 (PTAB December 14, 2015) (final written decision for U.S. Patent No. 7,881,150 B2), *Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-00883, Paper No 33 (PTAB December 14, 2015) (final written decision for U.S. Patent No. 8,081,536 B1), and *Diablo Techs., Inc. v. Netlist, Inc.*, Case IPR2014-01011, Paper No. 34 (PTAB December 14, 2015) (final written decision for U.S. Patent No. 7,881,150 B2).

[7] *Netlist, Inc. v. Inphi Corp.,* Case No. 2:09-cv-6900 (C.D. Cal.), *Netlist, Inc. v. Google, Inc.,* Case No. 4:09-cv-05718 (N.D. Cal.), and *Google, Inc. v. Netlist, Inc.*, Case No. 4:08-cv-04144 (N.D. Cal.), all stayed due to the reexamination proceedings of the '912, '537, and '274 patents.

We affirm-in-part the Examiner's decision to reject or not to reject claims 1–43, 45–50, 52–54, 56–58, 60–63, 67–71, 75, 77–93, 109–111, and 119–136.

Illustrative claims 7 and 21 read as follows with emphasis added:

7. [The memory module of claim l] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices mounted to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit mounted to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input control signals from the computer system, the set of input control signals comprising at least one row/column address signal, bank address signals,
and at least one chip-select signal, the set of input control signals corresponding to a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output control signals in response to the set of input control signals, the set of output control signals corresponding to the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a first command signal and the set of input control signals from the computer system by generating and transmitting a second command signal and the set of output control signals to the plurality of memory devices, the first command signal and the set of input control signals corresponding to the second number of ranks and the second command signal and the set of output control signals corresponding to the first number of ranks; and

a phase-lock loop device mounted to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register, *wherein the bank address signals of the set of input control signals are received by both the logic element and the register.*

21. [The memory module of claim 15] A memory module connectable to a computer system, the memory module comprising:

a printed circuit board;

a plurality of double-data-rate (DDR) memory devices coupled to the printed circuit board, the plurality of DDR memory devices having a first number of DDR memory devices arranged in a first number of ranks;

a circuit coupled to the printed circuit board, the circuit comprising a logic element and a register, the logic element receiving a set of input signals from the computer system, the set of input signals comprising at least one row/column address signal, bank address signals, and at least one chip-select signal, the set of input signals configured to control a second number of DDR memory devices arranged in a second number of ranks, the second number of DDR memory devices smaller than the first number of DDR memory devices and the second number of ranks less than the first number of ranks, the circuit generating a set of output signals in response to the set of input signals, the set of output signals configured to control the first number of DDR memory devices arranged in the first number of ranks, wherein the circuit further responds to a command signal and the set of input signals from the computer system by selecting one or two ranks of the first number of ranks and transmitting the command signal to at least one DDR memory device of the selected one or two ranks of the first number of ranks; and

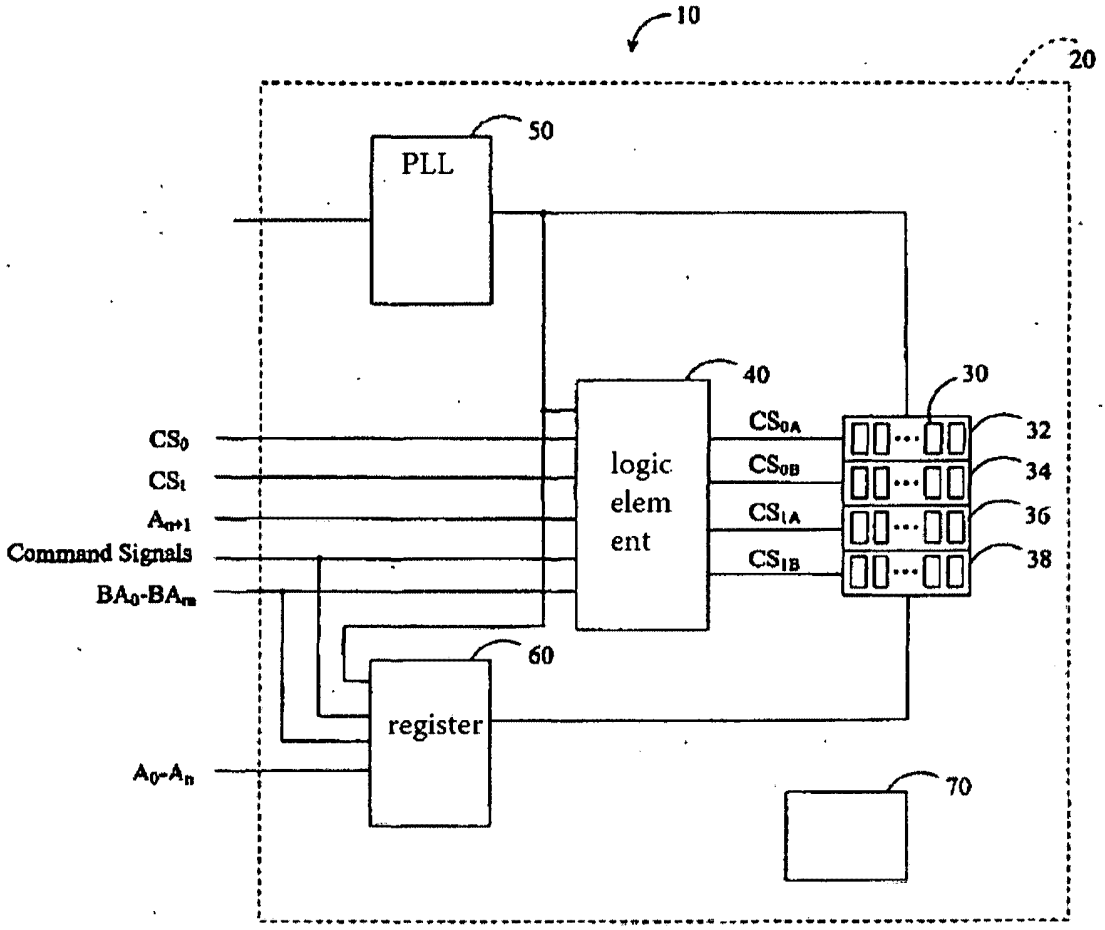
a phase-lock loop device coupled to the printed circuit board, the phase-lock loop device operatively coupled to the plurality of DDR memory devices, the logic element, and the register, *wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure.*

PO App. Br. 51–54, Claims App'x.[8]

[8] Underlining in claims indicates added language present in originally issued independent claims 1 and 15 respectively.

The Invention

The '912 patent illustrates an exemplary memory module 10 in Figure 1A below:



Annotated Memory Module illustrated in Figure 1A

The '912 patent 3:32–34, 5:6–8; Fig. 1. Memory module 10 contains printed circuit board 20. Memory devices 30, phase lock loop (PLL) 50, logic element 40, and register 60 are coupled to printed circuit board 20. The '912 patent 5:13–14, 22–27; Fig. 1A.

Memory devices 30 are a first number of memory devices (e.g., 4 DDR devices). The '912 patent 5:11–12, 6:12–16; Fig. 1A. The logic element 40

receives input control signals that correspond to a second number of memory devices smaller than the first number of memory devices (e.g., 2). The '912 patent 2:37–39, 5:14–20; Fig. 1A. Input control signals includes address signals, such as bank address signals (e.g., BA_0-BA_m), row address signals, column address signals, gated column address strobe signal, and rank or chip-select signals (e.g., CS_0 and CS_1), and command signals (e.g., refresh and precharge). The '912 patent 2:37–39, 6:56–61; Fig. 1A. Logic element 40 generates output control signals (e.g., CS_{0A}, CS_{0B}, CS_{1A}, CS_{1B}) in response to the input control signals, the output control signals corresponding to the first number of memory devices (e.g., 4). The '912 patent 5:18–21; Fig. 1A.

Additionally, in certain embodiments, the output control signals correspond to a first number of ranks (e.g., 4) in which the memory devices 30 are arranged. The '912 patent 6:55–67, 7:36–38. On the other hand, the input control signals correspond to a second number of ranks (e.g., 2) per memory module, for which the computer system is configured. The '912 patent 6:67–7:9, 7:20–29, 38–39; Fig. 1A. The second number of ranks is smaller than the first number of ranks. *See id.* In such a scenario, memory module 10 simulates a virtual memory module, and this may occur when the number of memory devices 30 of memory module 10 is larger than the number of memory devices 30 per memory module the computer system is configured to use. The '912 patent 7:9–19. This arrangement can improve memory module performance, capacity, or both. The '912 patent 1:21–24.

As shown above in Figure 1A, the bank address signals, $BA_0 - BA_m$, are received by both register 60 and logic element 40.

In addition, Figure 2B shows that logic element 40 can save or latch an input control signal (e.g., A_{13}) during a row access procedure (e.g., column access strobe (CAS) high) at program logic device (PLD) 42 and can transmit this signal as an output control signal during a subsequent column access procedure (e.g., CAS low). The '912 patent 21:54–66; Fig. 2A. Figure 2B illustrates this below:

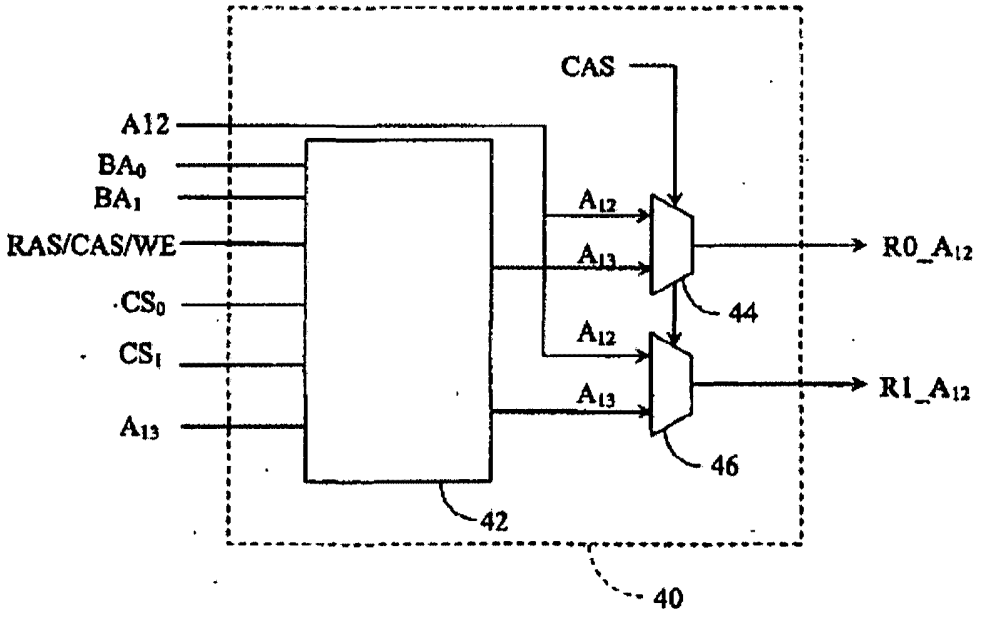


Figure 2B showing Logic Element 40 with PLD 42 Storing Signals

The '912 patent 3:44–45, Fig. 2B. In this exemplary logic element, ranks 32 and 34 (shown in Figure 2A) interpret the previously-saved row address (e.g., A_{13}) as a current column address (e.g., A_{12}), and logic element 40 translates the extra row address into an extra column address. The '912 patent 21:66–22:4; Fig. 2A–B.

Cited Prior Art

The Examiner relies on the following as evidence of unpatentability:

Connolly	US 5,745,914	Apr. 28, 1998
Dell (Dell 1)	US 5,926,827	July 20, 1999
Dell (Dell 2)	US 6,209,074	Mar. 27, 2001

Olarig	US 6,260,127 B1	July 10, 2001
Wong	US 6,414,868 B1	July 2, 2002
Dell (Dell 184)	US 6,446,184 B2	Sept. 3, 2002
Amidi	US 2006/0117152	June 1, 2006 (filed Jan. 5, 2004)

Miles J. Murdocca and Vincent P. Heuring, Principles of Computer Architecture (Chapter 7) 243–252 (2000) (Murdocca)

Micron, *DDR SDRAM RDIMM, MT36VDDF12872 - 1GB, MT36VDDF25672 - 2GB* 1–20 (2002) (Micron)

JEDEC Standard No. 21-C, *PC2100 and PC1600 DDR SDRAM Registered DIMM, Design Specification, Rev. 1.3* pages 4.20.4-1–4.20.4-82 (Jan. 2002) (JEDEC 21-C)

JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification JESD79C (Rev. of JESD79B) 1–75 (Mar. 2003) (JEDEC 79C)

JEDEC STANDARD, Definition of the SSTV16859 2.5 V 13-Bit to 26-Bit SSTL_2 Registered Buffer for Stacked DDR DIMM Applications, JESD82-4B (Rev. of JESD82-4A) 1–12 (May 2003) (JEDEC 82-4B)[9]

HP Printer Memory Explained 1–7 (Jan. 21, 2004), *available at* http://warshaft.com/hpmem.htm (Memory Explained)

The following Declarations are presented in this merged proceeding:

Declaration of Dr. Carl Sechen dated July 5, 2011 (Sechen Decl.),

Declaration of Dr. Carl Sechen dated January 13, 2013 (2d Sechen Decl.),

Declaration of Dr. David Wang dated August 29, 2011 (Wang Decl.),

Declaration of Dr. David Wang dated February 13, 2012 (2d Wang Decl.),

Declaration of Dr. David Wang dated February 13, 2013 (3d Wang Decl.),

[9] Notably, JEDEC 21-C, JEDEC 79C, and JEDEC 82-4B are often referred to collectively as JEDEC or JEDEC standards in the presented rejections, the briefs, and declarations. *See, e.g.*, Sechen Decl. ¶ 8.

Declaration of Dr. Nader Bagherzadeh dated August 25, 2011 (Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated February 10, 2012 (2d Bagherzadeh Decl.),

Declaration of Dr. Nader Bagherzadeh dated February 13, 2013 (3d Bagherzadeh Decl.),

Declaration of Dr. Christoforos Kozyrakis dated October 21, 2010 (Kozyrakis Decl.),

Declaration of Dr. Christoforos Kozyrakis dated August 28, 2011 (2d Kozyrakis Decl.),

Declaration of Dr. Christoforos Kozyrakis dated February 23, 2012 (3d Kozyrakis Decl.),

Declaration of Dr. Christoforos Kozyrakis dated February 13, 2013 (4th Kozyrakis Decl.), and

Declaration of Dr. Bruce Jacob dated October 19, 2010.

Adopted Rejections

Patent Owner appeals the following rejections adopted by the Examiner:

Reference(s)	Basis	Claims	RAN
Amidi (Ground 3[10])	§ 102	2, 5, 7, 9, 21, 23, 30, 33, and 119	11, 22–26

[10] Throughout the documents in this proceeding, the Examiner, Patent Owner and Requesters 1–3 refer to the various rejections by ground number. *See, e.g.*, RAN 11. We include the ground number here and in the Opinion.

Amidi (Ground 4)	§ 103(a)	2, 5, 7, 9, 21, 23, 30, 33, 57, and 119	12, 28
Amidi and Dell 2 (Ground 5)	§ 103(a)	2, 5, 7, 9, 21, 23, 26, 30, and 33	12, 30
Amidi and JEDEC (Ground 6)	§ 103(a)	7, 9, 21, 33, 57, and 119	12, 32–33
Dell 1 and JEDEC (Ground 9)	§ 103(a)	9 and 21	RAN 13, 36–39
Wong and JEDEC (Ground 11)	§ 103(a)	9 and 21	RAN 13, 41–43
Micron and Connolly (Ground 12)	§ 103(a)	7, 9, 21, 26, and 33	RAN 13, 44–47
Micron and Amidi (Ground 13)	§ 103(a)	7, 9, 21, 26, 33, and 57	RAN 14, 49–52
Micron, Amidi, and Dell 2 (Ground 19)	§ 103(a)	21	RAN 14, 55

PO App. Br. 11.

ISSUES ON APPEAL

We review the appealed rejections for error based upon the issues identified by Owner in its appeal brief, and in light of the arguments and evidence produced thereon. *Cf. Ex parte Frye*, 94 USPQ2d 1072, 1075 (BPAI 2010) (precedential) (citing *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992)). "Any arguments or authorities not included in the brief[s] permitted under this section or [37 C.F.R.] §§ 41.68 and 41.71 will be refused consideration by the Board, unless good cause is shown." 37 C.F.R. § 41.67(c)(1)(vii).

Based on the arguments and evidence presented by Owner, the main issues on appeal are whether the Examiner erred in determining:

(I) Amidi alone or in combination with at least one other reference (Grounds 3–6) disclose or teach:

(A) "the bank address signals of the set of input control signals are received by both the logic element and the register" recited in claim 7 and similarly recited in claims 26 and 33 (bank address limitation)?

(B) "wherein the circuit is configured to store an input signal of the set of input signals during a row access procedure for subsequent use during a column access procedure" recited in claim 21 and similarly recited in claims 2, 5, 23, and 30 (storing limitation)?

(II) Micron and Amidi (Ground 13) teach

(A) the bank address limitation recited in claim 7 and similarly recited in claims 26 and 33?

(B) the storing limitation recited in claim 21?

(III) the proposed rejections of certain claims should not be adopted?

ANALYSIS

Patent Owner's Appeal

Preliminary Matters

Patent Owner states it "is not appealing the rejections of claims 9 and 57." PO App. Br. 47; R3 Resp. Br. 1. These claims have been rejected under Grounds 3–6, 9, and 11–13. RAN 11–14. Because no arguments have been presented for these claims, we summarily sustain the rejections of these claims. *See Hyatt v. Dudas*, 551 F.3d 1307, 1314 (Fed. Cir. 2008) (explaining that when appellant fails to contest a ground of rejection, the Board may affirm the rejection without considering its substantive merits).

Claim Construction

During examination of a patent application, a claim is given its broadest reasonable construction "in light of the specification as it would be interpreted by one of ordinary skill in the art." *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (citations and internal quotation marks omitted). We presume that claim terms have their ordinary and customary meaning. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) ("The ordinary and customary meaning 'is the meaning that the term would have to a person of ordinary skill in the art in question.'") (internal citations omitted). However, patentees may rebut this presumption by acting as their own lexicographer, providing a definition of the term in the specification with "reasonable clarity, deliberateness, and precision." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994).

Claims 2, 5, 7, 21, 23, 26, 30, and 33 recite a circuit comprising "a logic element." The '912 patent states that logic element 40 in certain embodiments can be a PLD, an application-specific integrated circuit (ASIC), a field-programmable gate array (FPGA), a custom-designed semiconductor device, or a complex PLD (CPLD). The '912 patent 6:39–43. The '912 patent also describes the logic element in certain embodiments as "a custom device," "compris[ing] various discrete electrical elements," or being "one or more integrated circuits" in certain embodiments. The '912 patent 6:43–44, 48–52. As such, the '912 patent describes "a logic element" in expansive terms, but none of the above passages define or limit the meaning of "logic element" with sufficient precision.

The Examiner similarly determines the '912 patent has not defined "a logic element" and further finds this phrase is not a term of art. RAN 69. The Examiner thus construes the phrase "logic element" to have its plain meaning to include "an element that performs some kind of logic function or an element that comprises a logic circuit." *Id.* Requester 1 proposes that one skilled in the art would have understood a logic element "to mean any circuit that implements one or more logic functions using combinational or sequential logic functions. [*See* Declaration of David Wang, Ph.D., filed Aug. 29, 2011 ("1st Wang Decl.", attached as Exhibit B-1) at ¶¶ 7, 30]." R1 Resp. Br. 5. Requester 2 also proposes an interpretation of "logic element," urging that is "at least as broad" as Patent Owner proposed in litigation. R2 Request 22 (citing R2 Request, Evid. App., Ex. OTH-C 7). In that context, Patent Owner urged "a logic element" to mean a "hardware circuit that performs a predefined function on input signals and presents the resulting signal as its output." *Id.*

Given the record and that the '912 disclosure fails to define the term, we accept the Examiner's understanding of "a logic element" as reasonable, which includes "an element that performs some kind of logic function or an element that comprises a logic circuit." RAN 69. This understanding is consistent with the expansive discussion in the '912 patent that includes a "custom device" or a generic device comprising "various discrete electrical elements." The '912 patent 6:43–44, 48–50.

The Examiner also states "there is nothing in the claims or the specification that precludes the logic element from comprising a storage device such as a register." RAN 69. Notably, each of claims 2, 5, 7, 21, 23, 26, 30, and 33 recites "a register" separate from "a logic element." This distinction in claim language

presumably supports that the recited "logic element" is something different from a register. Both the Examiner and Dr. Sechen also note they "are separate elements in the claims." RAN 69, 74; Sechen Decl. ¶ 20. Dr. Sechen further argues that one skilled in the art "would understand that the term 'logic element' implies something inherently different than the term 'register.'" Sechen Decl. ¶ 19.

We agree that the recited "logic element" is distinct element from the recited "register." RAN 69, 74. However, the expansive examples in the '912 patent of a logic element cover custom devices or a device of various discrete electrical components, which includes at least some types of registers. Requester 1 also provides the testimony of Dr. Wang, supporting that a register performs logical operations and is a logical element. R1 Resp. Br. 5 (citing Wang Decl. ¶ 7). That is, Dr. Wang testifies that "[r]egisters are logic elements," because they implement one or more logic functions (e.g., AND, NAND, OR, NOR, etc.). Wang Decl. ¶ 7. Also, even Dr. Sechen, Patent Owner's own expert, admits that a register includes "a small amount of control logic" (Sechen Decl. ¶ 19), indicating that registers perform some type of logic function or comprise a logic circuit.

Accordingly, we determine that a reasonably broad interpretation of "a logic element," in light of the '912 patent's disclosure and the testimony of what one of ordinary skill in the art would have understood, includes custom devices and devices with various discrete electrical components that implement logic operations, including registers. We further determine the recited "logic element" is also not limited to a single component, given that the disclosure states the logic element can comprise various discrete electrical components.